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(54) A semiconductor device and method of manufacture.

(57) A semiconductor substrate (3) is utilised to integrally form a drive circuit (8) and a pixel array (9) to produce a transparent semiconductor device for a light valve.

The semiconductor device for a light valve is constructed by the semiconductor substrate (3) having an opaque portion (1) and a thin transparent portion (2). The pixel array (9) is formed in the transparent portion. The drive circuit (8) is formed in a top face of the opaque portion (1). A transparent support substrate (5) is laminated to the top face of the semiconductor substrate (3) for reinforcement. A bulk of the semiconductor substrate (3) is removed from a back face by selective etching to provide the transparent portion (2).

FIG. 1 (A)

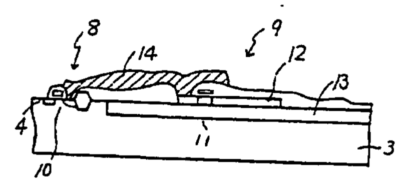


FIG. 1 (B)

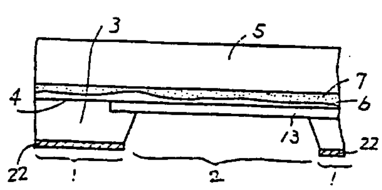
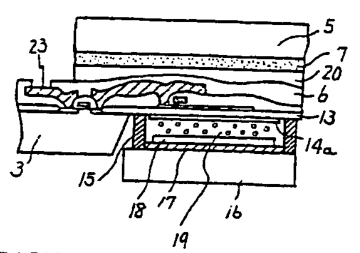


FIG. 1 (C)



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The present invention relates to a semiconductor device for a light valve and a production method thereof. More specifically, but not exclusively, the present invention relates to a transparent semiconductor device and method of manufacture of such a transparent semiconductor device for use as driving substrate of a flat light valve such as an active matrix liquid crystal display device.

Figure 26 shows a general construction of a typical driving substrate used in an active matrix liquid crystal display device. The driving substrate 1001 has formed integrally thereon, a pixel array 1002 and a peripheral drive circuit including an X-drive 1003 and a Y-drive 1004 by known integrated circuit (IC) fabrication processes.

Figure 27 schematically shows the pixel array in more detail. A thin film transistor (TFT) 1007 is arranged to switch a pixel 1008 at each intersection between plural scan lines 1005 and plural signal lines 1006. The TFT 1007 is connected at its gate electrode to a corresponding scan line 1005, connected at its source electrode to a corresponding signal line 1006, and connected at its drain electrode to a corresponding liquid crystal pixel 1008. The liquid crystal pixel 1008 is composed of a liquid crystal layer sandwiched between the driving substrate and a counter substrate. While the scan lines 1005 are scanned to select and open the TFTs 1007, the signal lines 1006 are accessed to write an image signal into the corresponding liquid crystal pixels 1008.

The TFT is composed of a semiconductor thin film material conventionally selected from polysilicon or amorphous silicon. However, these materials have a relatively low mobility. Hence, it would be difficult to utilise the TFT for a transistor element of the peripheral drive circuit. In view of this, another technology has been developed recently such that a single crystal silicon (monosilicon) transistor is formed to constitute a peripheral drive circuit element, as disclosed for example in Japanese Patent Publication No. 3-100516 (Tokkaihei). This prior art utilises a composite substrate comprised of a monosilicon wafer laminated on another wafer composed of a transparent insulating material such as quartz glass. The monosilicon wafer is partly removed by etching so that a pixel array is formed on an exposed surface of the quartz glass wafer, while a peripheral drive circuit is formed in the remaining part of the monosilicon wafer.

However, when a high temperature IC process, over 1000°C, is applied to the composite substrate comprised of a laminate of the quartz glass wafer and a monosilicon wafer, the substrate is deformed due to the thermal expansion difference. This disadvantageously hinders the yield rate and reliability. In view of the aforegoing, an object of the present invention is to construct a semiconductor device for a light valve by using a stable substrate free thermal deformation.

According to the present invention, there is provided a semiconductor device for a light valve comprising

a substrate having an opaque portion and a transparent portion,

a pixel formed on the transparent portion,

a drive circuit formed on the opaque portion for driving the pixel, characterised by

a transparent support substrate laminated to the substrate over at least the pixel.

The solution to the above noted problem of the prior art and to achieve the object of the present invention will now be described with reference to figure 1.

First, as shown in figure 1(B), the inventive semiconductor device for a light valve is formed of a semiconductor substrate 3 having an opaque portion 1 of a certain thickness, and a transparent portion 2 free of said thickness. The semiconductor substrate in the opaque portion has a thickness sufficient to prevent light transmitting. Typically, over 10μm in thickness.

The semiconductor substrate 3 is composed of a bulk monosilicon (single crystal silicon) wafer. A pixel array is formed in the transparent portion 2 along a major face 4 of the semiconductor substrate 3, while a drive substrate is formed in the opaque portion 1 along the same major face 4.

Further, a transparent support substrate 5 composed of, for example, quartz glass is superposed on the major face 4 of the semiconductor substrate where the pixel array and the drive circuit are provided.

Preferably, the support substrate 5 is bonded to the semiconductor substrate 3 through a protective film 6 and an adhesive layer 7. The transparent support substrate 5 can be constituted by the adhesive layer 7 itself or both the adhesive layer 7 and a levelling layer (not shown in figure 1) which is interposed between the adhesive layer 7 and the protective layer 6.

An incomplete form of the semiconductor device shown in figure 1(B) is illustrated in figure 1(A). As described before, a high temperature IC process is applied to the semiconductor substrate 3 to form concurrently the drive substrate 8 and the pixel array 9. In this construction, the drive circuit 8 contains a single crystal transistor 10 formed directly in the major face 4 of the semiconductor substrate 8. The pixel array 9 contains a switching element in the form of a TFT 11 and a pixel electrode 12. This pixel array 9 is formed on an underlying insulative film 13 provisionally provided along the major face 4 of the semiconductor substrate 3. The pixel array 9 and the drive circuit 8 are interconnected to each other through a metal lead 14 on the same substrate.

Figure 1(C) shows an active matrix liquid crystal display device constructed of the semiconductor device shown in figure 1(B) for a light valve. The liquid crystal display device is constructed by using a cavity

formed in the transparent portion of the semiconductor substrate 3. An orientation film 14a is formed on the back of the underlying insulative film 13 exposed in the transparent portion. Further, a transparent counter substrate 16 is laminated through a spacer 15 composed of a seal material. A common electrode 17 and an orientation film 18 are formed on an inner face of the counter substrate 16. A liquid crystal layer 19 is filled between the orientation films 14a and 18. Though not shown in figure 1(B), a levelling layer 20 is preferably interposed between the protective film 6 and the adhesive layer 7. Further, a periphery of the transparent support substrate 5 is partly removed to expose an electrode terminal for external connected (pad electrode) 23.

The description will now turn to a production method of the inventive semiconductor device for a light valve again with reference to figure 1. As shown in figure 1(A), the first step is to form the pixel array 9 and the drive circuit 8 on the major face 4 of the semiconductor substrate 3. Since the semiconductor substrate 3 is composed of, for example, a bulk monosilicon wafer, a high temperature IC process is directly applied in a manner similar to regular LSI fabrication technology. Further, the TFT 11 contained in the pixel array 9 and the single crystal transistor 10 contained in the drive circuit 8 can be fabricated by the same process. In this first step, the underlying insulative film 13 is provisionally formed under the pixel array 9, and will serve as an etching stopper in a later step. The underlying insulative film 13 is composed of, for example, a silicon oxide film, a silicon nitride film or a composite film thereof.

Next, as shown in figure 1(B), the second step is to bond the transparent support substrate 5 to the major face 4 of the semiconductor substrate 3 by means of the adhesive layer 7. The transparent support substrate 5 is composed of, for example, glass, quartz or sapphire, and preferably has a thermal expansion coefficient comparable to that of the semiconductor substrate 3. Further preferably, the levelling layer 20 is interposed between the transparent adhesive layer 7 and the semiconductor substrate 3 to compensate for any unevenness of the major face. Although the transparent support substrate 5 is adhered over the whole portion of the major face on which the drive circuit 8 is formed, as shown in figure 1(B), the transparent support substrate 5 alternatively can be bonded adhesively over the transparent portion 2 and only slightly covering the opaque portion 1. This is because the pixel array 9 in the transparent portion 2 has to maintain the mechanical strength in the third step of making the pixel array transparent. Preferably, the extent of overlap of the transparent support substrate 5 over the opaque portion 1 is larger than the thickness of both the opaque portion 1 and the semiconductor substrate 3. In this case, the semiconductor substrate 3 acts as reinforcing the substrate in the opaque portion 1.

Subsequently, the third step involves selectively removing a thickness of the semiconductor substrate 3 over a region of the pixel array from the back face opposite to the major face 4, thereby making the pixel array transparent. The third step is carried out by etching using a resist mask 22 and using the underlying insulative film 13 as the etching stopper as described before. The semiconductor device for a light valve is thus produced by such a manner. Further, as shown in figure 1(C), a liquid crystal cell can be assembled into the transparent portion from which the thickness or bulk of the semiconductor substrate is removed.

The present invention utilises a bulk semiconductor substrate, and the drive circuit and the pixel array are integrally formed by a regular IC process. In contrast to the prior art which uses a composite substrate, the semiconductor substrate will not suffer from thermal deformation under high temperature processing, thereby producing the semiconductor device for a light valve featuring a compact size, high resolution and large capacity. The drive circuit is comprised of a single crystal transistor thereby achieving faster and higher operation characteristics as compared to the prior art.

The semiconductor substrate formed with the drive circuit and the pixel array is reinforced by the transparent support substrate along its major face, while the thickness or bulk of the semiconductor substrate is etched away to make the substrate transparent. This etching process is applied to the back face of the substrate to avoid contamination and destruction of any of the elements involved in the drive circuit and the pixel array to thereby ensure device reliability. Further, the semiconductor substrate is reinforced by the transparent support substrate for ensuring mechanical strength while a window is opened for a display in the semiconductor substrate. Moreover, a liquid crystal cell or other device can be mounted compactly in the display window from which the thickness of the semiconductor bulk is removed. Furthermore, since the portion formed with the drive circuit has the grater thickness or bulk of the semiconductor substrate, any heat generated by the drive circuit can be absorbed immediately, so that the drive circuit can operate stably whilst suppressing any temperature fluctuations and in particular temperature rises. In this case, the thickness of the semiconductor substrate is preferably more than 100μm.

Embodiments of the present invention will now be described with reference to the accompanying drawings, of which:

Figures 1(A) to 1(C) are schematic diagrams showing a basic concept of the inventive semiconductor device for a light valve and the production method thereof;

Figures 2(A) and 2(B) are schematic sectional di-

agrams showing an embodiment of a TFT which constitutes a pixel switching element;

Figure 3 is a schematic sectional diagram showing an embodiment where a liquid crystal cell is assembled into a top face of the inventive semiconductor device for a light valve;

Figures 4(A) to 4(C) are production step diagrams of the figure 3 embodiment;

Figure 5 is a schematic partial sectional diagram showing another embodiment of the inventive semiconductor device for a light valve;

Figure 6 is a schematic diagram showing a light shielding structure of a TFT which constitutes a pixel switching element;

Figure 7 is a schematic diagram showing another light shielding structure of a TFT;

Figure 8 is a schematic diagram showing a further light shielding structure of a TFT;

Figure 9 is a schematic diagram showing a still further light shielding structure of a TFT;

Figure 10 is a schematic diagram showing another light shielding structure of a TFT;

Figures 11(A) to 11(G) are diagrams showing IC processes involved in the inventive production method of the semiconductor device for a light valve;

Figures 12(A) to 12(G) are diagrams showing a second example of the IC process;

Figures 13(A) to 13(G) are diagrams showing a third example of the IC process;

Figures 14(A)to 14(F) are diagrams showing a fourth example of the IC process;

Figure 15 is a diagram illustrating a pad being formed to a counter electrode;

Figures 16(A) to 16(D) are diagrams showing a fifth example of the IC process;

Figure 17 is a diagram showing a sixth example of the IC process;

Figures 18(A) and 18(B) are diagrams showing a first example of an etching process from a back face which is part of the inventive production method of the semiconductor device for a light valve;

Figures 19(A) to 19(C) are diagrams showing a second example of the etching process;

Figure 20 is a diagram showing a third example of the etching process;

Figures 21(A) and 21(B) are diagrams showing a fourth example of the etching process;

Figures 22(A) to 22(C) are diagrams showing a fifth example of the etching process;

Figures 23(A) to 23(D) are diagrams showing a sixth example of the etching process;

Figures 24(A) and 24(B) are diagrams showing a seventh example of the etching process;

Figures 25(A) to 25(D) are diagrams showing an eighth example of the etching process;

Figure 26 is a schematic plan view showing a driving substrate of a conventional active matrix liquid crystal display device; and

Figure 27 is a schematic structural diagram of a pixel array formed in the conventional drive substrate.

Preferred embodiments of the present invention will now be described in detail with reference to the drawings.

Figure 2 is a schematic sectional diagram showing one embodiment of a switching element involved in the pixel array. In this embodiment as shown in figure 2(A), the pixel switching element is comprised of a polysilicon TFT 25. In more detail, a polysilicon thin film 27 is provided in a predetermined pattern on an underlying insulative film 26. A pair of source region S and drain region D are formed in one part of the polysilicon thin film 27 in the form of a high density impurity region. A gate electrode G is patterned on a channel region disposed between both of the regions S, D, and is disposed through a gate insulating film 29a. Another part of the polysilicon thin film 27 is extended to form a pixel electrode 28.

Preferably, the thickness of the pixel electrode is set in the range of 50nm ± 10nm to effectively obtain optimum balance transmissive characteristics for three primary colour (RGB) incident lights. Such a structure of the TFT 25 and the pixel electrode 28 is coated by an intermediate insulating film 29. Further, a metal lead 30 composed of aluminium or other such material, to the TFT through a contact hole opened in the intermediate insulating film 29. A part of the metal lead 30 covers an active region of the TFT 25 to function as light shielding film. Though the TFT is composed of the polysilicon thin film in this embodiment, the present invention may not be limited to such a structure. Alternatively, an amorphous silicon thin film or single crystalline silicon thin film may be used in place of the polysilicon thin film. Further, the switching element may be comprised of a diode in place of the TFT.

Figure 2(B) shows a variation of the TFT shown in figure 2(A). In this variation, a section of the pixel electrode 28 is thinned exclusively in the order of 50nm to selectively achieve transparency in the patterned polysilicon thin film 27. On the other hand, the remaining section of the polysilicon thin film 27 has a sufficient thickness to provide an active region of the TFT 25 so as to improve the transistor performance.

Figure 3 is a schematic sectional diagram showing one embodiment of the inventive semiconductor device for a light valve. A semiconductor substrate 31 is divided into a opaque portion 32 having a certain bulk thickness, and a transparent portion 33 from which the bulk thickness is removed. A drive circuit (not shown) is formed in a major face 34 of the semiconductor substrate 31 within the opaque portion 32. Preferably, the semiconductor substrate 31 in the

opaque portion 32 has a thickness sufficient to prevent light transmittance: eg. over 10μm in thickness. Furthermore, if the thickness of the semiconductor substrate 31 in the opaque portion 32 is over 100μm then this obviates any temperature increase caused by heat generated in the drive circuit. On the other hand, a pixel array is formed on an underlying insulative film 35 within the transparent portion 33. The pixel array contains a switching element in the form of a TFT 36. The semiconductor substrate 31 is bonded to a transparent support substrate 38 by means of a sealer 37 for reinforcement. In this embodiment, the transparent support substrate 38 is placed in registration with the transparent portion 33 or display window portion to serve as a counter substrate. Namely, a liquid crystal layer 39 is filled between the underlying insulative film 35 and the counter substrate 38 to constitute a liquid crystal cell. Further, the underlying insulative film 35 is supported by the filled liquid crystal layer 39 and one or more spacers 40. The spacer 40 is provided just over the TFT 36 to improve a pixel open rate.

Although the liquid crystal cell is of an active matrix type in this embodiment, the present invention is not limited to such a construction. Alternatively, a simple matrix structure may be adopted in place of the active matrix structure, which only has stripes of transparent pixel electrodes. Further, a transparent resin may be filled in the display window portion from which the bulk thickness is removed for reinforcement of the transparent portion 33. In addition, a second transparent support substrate may be bonded adhesively for reinforcement onto the transparent portion 33.

Figure 4 is a diagram showing a production method of the figure 3 device in which the liquid crystal cell is disposed on the top major face. Figure 4 shows when a polysilicon TFT is used as a switching element in the pixel array. In a first step shown in figure 4(A), an IC process is applied to a top major face of a semiconductor substrate 41 composed of a bulk single crystal silicon to form a peripheral drive circuit and a pixel array. In this embodiment, the peripheral drive circuit contains a regular silicon single crystal transistor 42 which is directly and integrally formed in the major face of the semiconductor substrate 41. On the other hand, the pixel array is formed on a transparent insulating film 43 which is obtained by surface LOCOS oxidation of the semiconductor substrate 41. This pixel array includes a polysilicon TFT 44 and a pixel electrode 45 which is formed in an extended part of a drain region of the TFT 44. Those of the silicon transistor 42 and the polysilicon TFT 44 are coated by an intermediate insulating film 46 composed of PSG or else. Lastly, a contact hole is opened through the intermediate insulating film 46, a metal lead 47 is formed, and a thin protective film or passivation film 48 is coated thereover. Subsequently, the fabrication step switch to the back face so that a portion where the peripheral drive circuit is provided is selectively covered by a resist mask 49 composed of silicon nitride or else having a certain etching resistance. The resist mask 49 is patterned by, for example, a two-face aligner.

In the next step shown in figure 4(B), a transparent support substrate 51 is bonded to the top face of the semiconductor substrate 41 by means of a sealer 50. Prior to this step, an orientation film 52, made of polyimide or else, is formed on a surface of the pixel array. On the other hand, a counter electrode 53 and another orientation film 54, made of polyimide, are provisionally formed on an inner surface of the transparent support substrate 51. After the semiconductor substrate 41 and the transparent support substrate 51 are laminated to each other, liquid crystal is filled in a gap between both of the substrates to form a liquid crystal layer 55. Further a support post or spacer 56 is provisionally provided on top of each TFT 44 by means of screen printing or other methods.

In the last step shown in figure 4(C), the semiconductor substrate 41 is etched through the resist mask 49 to remove the bulk thickness just under the pixel array to make the same transparent. This etching process utilises an alkali etchant such a KOH solution. An end point of the etching process is automatically determined by the underlying insulative film 43 functioning as an etching stopper. Components on the top face are eliminated from the view of the figure 4(C) for clarity.

Figure 5 is a partial sectional diagram schematically showing an opaque portion 61 of another embodiment of the semiconductor device for a light valve according to the present invention. A semiconductor substrate 62 is formed with a drive circuit in the surface, comprised of a silicon transistor 63 of an insulating gate field effect type. Individual transistors 63 are separated from each other by a field oxide film 64. A metal lead 66 and a pad electrode 67 electrically connected thereto, are provided for external coupling and are formed in a given pattern over an intermediate insulating film 65. Further, the drive circuit except for the pad electrode 67 is coated by a passivation film 68. A transparent support substrate 69, composed of glass or else, is bonded to the semiconductor substrate through an adhesive layer 70. Preferably, the adhesive layer 70 is composed of a silicondioxide paste which will be cured by heating or ultraviolet ray irradiation. Further, a levelling layer 71 is interposed between the adhesive layer 70 and the passivation film 68. Preferably, the levelling layer 71 is also composed of silicondioxide material sufficient for significantly absorbing any surface unevenness of the semiconductor substrate 62.

In this embodiment, the transparent support substrate 69 is removed partly over the pad electrode 67 thereby facilitating external connection. In order to re-

move partly the transparent support substrate 69, after an individual semiconductor device for light valve is cut out by a scriber at a line indicated by the arrow, a part of the transparent support substrate 69 is selectively separated along a line indicated by the reverse triangle mark. An end part of the transparent support substrate 69 to be cut away is provisionally formed with an undercut effective to avoid contact with the pad electrode 67. Although the transparent support substrate 69 is formed over the drive circuit as shown in figure 5, the transparent support substrate 69 may of course, not be formed covering the drive circuit but only covering the opaque portion 61.

Description will now be given for various embodiments with regard to a light shielding structure of TFT in conjunction with figures 6 to 10. Generally, the TFT used for a pixel switching element has a tendency to increase leak current upon irradiation by an incident light. To compensate for this, it is expedient to add an adequate light shielding structure when utilising the TFT in the semiconductor device used for a light valve.

Figure 6 shows a first example of a light shielding structure. A pixel switching element is provided in the form of a TFT 82 on an underlying insulative film 81. The TFT 82 is comprised of a source region S and a drain region D formed in a thin polysilicon film 83, and a gate electrode G formed over a gate insulating film (not shown). A light shielding film 84 is disposed on a back face of the underlying insulative film 81, and is patterned in registration with an active region of the TFT 82. The light shielding film 84 may be composed of a high melting point metal, a silicide or a silicon.

Figure 7 shows a second example of a light shielding structure. An electrically conductive light shielding film 92 is formed on a top face of an underlying insulative film 91 in a given pattern. A thin insulating film 93 is provided to cover the light shielding film 92. Further, a patterned polysilicon is formed over the film 93 to provide a TFT 95 for a pixel switching element in a manner similar to the previous example. In this example, the electrically conductive light shielding film 92 is disposed just under a channel region of the TFT 95 through the thin insulating film 93 to thereby function as a "back gate electrode".

Figure 8 shows a third example of a light shielding structure. A TFT 102 is formed on an underlying insulative film 101 in a manner similar to the other examples. A patterned metal lead 104 is formed thereover through an intermediate insulating film 103, and is electrically connected to a source region of the TFT 102. A part of this metal lead 104 is extended to cover an active region of the TFT 102 to thereby function as a light shielding film.

Figure 9 is a schematic sectional diagram showing a fourth example of a light shielding structure. This example is a combination of the light shielding constructions shown in figures 6 and 8. Namely, a TFT 111 is shielded from the top and bottom to thereby almost perfectly suppress any photo-leak current. An upper light shielding film is composed of a part of a metal lead 112, and a lower light shielding film is composed of a pattern film 114 formed on a back face of an underlying insulative film 113 in registration with the TFT 111.

Figure 10 is a schematic sectional diagram showing a fifth example of a light shielding structure. This example is a combination of the light shielding structures shown in figures 7 and 8 such that a TFT 121 is almost completely shielded from above and below. An upper light shielding film is composed of a part of a metal lead 122, while a lower light shielding film is composed of an electrically conductive pattern film 123 which functions also as a back gate electrode.

Description is now given for the production method of a semiconductor device for a light valve according to the present invention. Figure 11 shows when a polysilicon TFT is used as a switching element in the pixel array.

The production method is generally divided into two steps.

In a first step, an IC process is applied to a semiconductor substrate to form a pixel array and a drive circuit. In the succeeding step, the semiconductor substrate is selectively etched to achieve transparency. Hereinafter, example of the IC process will be described with reference to figures 11 to 17. Further, examples of the etching process or transparency process will be described with reference to figures 18 to 25. Thereafter described various initial and succeeding steps can be effected in a different manner to the order described and may be selected according to structure, material and usage of the semiconductor device for a light valve.

Initially referring to figure 11, a first example of the IC process will be explained. This example utilises a bulk single crystal silicon (monosilicon) substrate. In step A, a field oxide film 131 is formed on a surface of a silicon substrate S for device isolation. Concurrently, an impurity is doped into a well to provide a device region, or field doping is also carried out. Further, a resist mask composed of a silicon nitride or else is provisionally formed on a back face of the silicon substrate S. Next in step B, a thin oxide film 133 is formed on a surface of the device region 132. Then, in step C, a polysilicon thin film 134 is formed on a surface of the field oxide film 131 in a given pattern, and thereafter the thin oxide film 133 is removed to make clean the device region 132. In a later step, a TFT is formed for pixel switching in the polysilicon thin film 134. Further, the field oxide film 131 just under the polysilicon thin film 134 will serve as an etching stopper in a later step. Then in step D, a gate insulating film 135 is concurrently formed on both of the device region 132 and the polysilicon thin film 134. Concurrently, channel doping is carried out. In

step E, individual gate electrodes 136 are formed in a given pattern over the device region 132 and the polysilicon thin film 134 through the gate insulating film 135. Further an impurity is introduced by ion implantation in self-alignment manner using each gate electrode 136 as a mask to thereby form a source region S and drain region D.

In such a manner, this example is advantageous in that the substrate is concurrently formed with those of a silicon transistor 137 which constitutes a drive circuit element and a polysilicon TFT 138 which constitutes a pixel switching element. In addition, a pixel element can be formed of the same polysilicon thin film concurrently with the TFT 138. Subsequently in step F, an intermediate insulating film 134 composed of PSG or else is entirely deposited over the silicon substrate S. Then, contact holes are formed through an intermediate insulating film 139 in communication with source and drain regions of the silicon transistor 137 and with a source region of the TFT 138. Lastly in step G, a metal lead film 140 is formed on the intermediate insulating film 134 in a given pattern.

Then, a passivation film 141 is coated. At this stage, the passivation film 141 is patterned so as to expose a pad electrode 142 for external connection. Thereafter, after bonding adhesively the transparent support substrate (not shown), the processing advances to the succeeding steps for the etching process. As described before, the field oxide film 131 over which the pixel array including the TFT 138 is formed, serves as an etching stopper. The field oxide film 131 has a thickness normally in the range of 0.5-1.0μm.

Figure 12 is a schematic step diagram showing a second example of the IC process. A pixel array will be formed on a right half portion of the figure, and a drive circuit will be formed on a left half portion of the same figure. First in step A, a field oxide film 151 is formed on a surface of a bulk single crystal silicon substrate S. Basically, the step is similar to step A of the first example shown in figure 11; however, this step is different in that a field oxide film is not formed in a portion where a pixel array is to be formed. Then in step B, a thin oxide film 152 is formed on an exposed surface of the silicon substrate S. Subsequently in step C, a silicon nitride film 153 is formed on the right half portion. Further, a silicon oxide film 154 is formed entirely over the silicon substrate S. This silicon oxide film 154 is provided to ensure junction stability relative to a later formed TFT as well as to improve adhesion. In step D, a polysilicon thin film 155 is formed in a given pattern over the silicon oxide film 154. Subsequently the previously formed thin oxide film 152 is removed from the device region 156. In step E, a gate oxide film 157 is formed over both of the device region 156 and the polysilicon thin film 155. Subsequently in step F, respective gate electrodes 158 are formed. Then, an impurity is doped by ion implantation to form a source region S and drain region D.

By such manner, a regular silicon transistor 159 is formed in the device region 156, and a TFT 160 and a pixel electrode are formed in the polysilicon thin film 155. In a manner similar to figure 11, the present method features that both of the drive circuit portion and the pixel array portion can be subjected concurrently to various treatments such as the gate oxide film forming process of a transistor, the channel doping process, the gate electrode forming process, and the impurity doping process for forming source/drain regions.

Lastly, in step G, a surface of the silicon substrate S coated with an intermediate insulating film 161. Thereafter, a metal lead 162 is formed in a given pattern. Further, a passivation film 163 is coated. After bonding adhesively the transparent support substrate, the processing is switched to the back face of the substrate to make the silicon substrate S transparent. In this case, an etching stopper is provided in the form of a composite film composed of the previously formed oxide film 152 and nitride film 153.

In contrast to the field oxide film shown in figure 11, this composite film is significantly thin, thereby improving driving efficiency when a liquid crystal cell or other device is assembled on the back face of the substrate.

Figure 13 is a step diagram showing a third example of the IC process. First in step A, a field oxide film 171 is formed over a bulk single crystal silicon substrate for device isolation. In a manner similar the first example shown in figure 11, the field oxide film 171 is provided entirely to cover a portion where a pixel array is to be formed in this example. In step B, an underlying silicon nitride film 172 is formed in a given pattern over the field oxide film 171 within the portion assigned to a pixel array. At this stage, the nitride film 172 is partly removed for electrode connection in advance. Further, a thin oxide film 174 is formed on a surface of each device region 173 within another portion where a drive circuit is to be formed. In step C, a silicon oxide film 175 is grown over the nitride film 172. A polysilicon thin film 176 is formed in a given pattern over the film 175. By interposing the oxide film 175, the condition of the junction to the polysilicon thin film 176 can be improved as well as improving the adhesion characteristic. Further, the thin oxide film 174 left on the device region 173 is removed. In step D, a gate oxide film 177 is formed concurrently on both of the polysilicon thin film 176 and the device region 173. Further, channel doping is also carried out concurrently for both the portions. In step E, gate electrodes 178 are formed concurrently in both the portions, and then ion implantation is conducted using the gate electrode as a mask to form concurrently a source region S and a drain region D.

By such a manner, a transistor 179 is formed in

the device region 173 for construction of a driver circuit, and a TFT 180 is formed in the polysilicon thin film 177 for pixel driving. Next in step F, an intermediate insulating film 181 is deposited over the silicon substrate S. A patterned metal lead film 182 is formed thereover so as to achieve electrical connection among the transistor elements through contact holes provided in the intermediate insulating film 181. At this stage, another metal lead 182 is formed in registration with the section 183 from which the nitride film 172 has been provisionally removed to thereby provide a pad for electrical connection to a counter electrode. Further, a passivation film 184 is coated entirely to protect the semiconductor device. However, the metal lead film 182 is locally uncoated so as to expose a section assigned to the pad electrode. After bonding the transparent support substrate on to the surface with the transistor 179 and TFT 180, the processing is switched to a back face of the substrate to etch away a bulk of the silicon substrate S to make the pixel array portion transparent. For example, KOH solution is used as an etchant and the field oxide film 171 serves as an etching stopper. Lastly in step G, an etchant is switched to hydrofluoric acid solution to etch away the field oxide film 171 and the intermediate insulating film 181 from exposed parts. At this stage, the intermediate insulating film 181 composed of PSG or else is etched away by self alignment through the open section 183 free of the nitride film 172 so that the metal lead 182 is exposed to the back face for connection to a counter electrode. A liquid crystal cell may be assembled in the display window portion formed by the removal of the bulk of the silicon substrate. In such a case, a counter electrode formed on a counter substrate is electrically connected to the exposed metal lead 182. In this embodiment, the field oxide film 171 is removed from the transparent portion. Hence a pixel electrode composed of the polysilicon thin film 176 can be disposed close to a liquid crystal layer filled in the liquid crystal cell.

Figure 14 is a schematic step diagram showing a fourth example of the IC process. A drive circuit will be formed in a left half portion of the figure, and pixel array will be formed in a right half portion of the same figure. In this example, a SOI substrate is utilised in place of the semiconductor substrate composed of a bulk single crystal silicon. The SOI substrate is constructed such that a monosilicon layer is laminated on a monosilicon wafer through a buried insulating film BOX. In constrast to a conventional composite substrate in which a quartz glass wafer and a monosilicon wafer are laminated with each other, the SOI substrate is composed of the same silicon material for the upper and lower layers interposed with the insulating film. Consequently, there is no substantial difference in thermal expansion coefficients for withstanding any high temperature process.

First, in step A, a monosilicon layer 191 is provided on the insulating film BOX and is partly etched to expose the insulating film BOX within a portion where the pixel array is to be formed. A well is formed in the monosilicon layer 191 which is left within another portion where the drive circuit is to be formed. In step B, a patterned polysilicon thin film 192 is formed over the exposed insulating film BOX. Subsequently in step C, LOCOS process is applied to the monosilicon layer 191 to form a field oxide film 193 for device isolation. In step D, a gate oxide film 195 is formed over both of the device region 194 and the polysilicon thin film 192. Further, channel doping is conducted to regulate threshold levels. Subsequently in step E, a patterned gate electrode 196, composed of a polysilicon or else, is concurrently formed on both of the device region 194 and the polysilicon thin film 192 through the gate oxide insulating film 195. Further, ion implantation is conducted in self alignment manner using the gate electrode 196 as a mask so as to dope a desired impurity to thereby form a source region S and a drain region D.

By such a manner, a transistor 197 is formed in the device region 194 for a drive circuit, while a TFT 198 for pixel switching is formed in the polysilicon thin film 192. Further, an extended section of the drain region D of the pixel switching TFT 198 constitutes a pixel electrode. Lastly in step F, the insulating film BOX formed thereon with the transistor elements is covered by an intermediate insulating film 199. A metal lead film 200 is formed over the film 199. Further, a passivation film 201 is deposited on the film 200. After bonding adhesively a transparent support substrate onto the surface with the transistors, the processing is switched to a back face of the substrate. The present example utilises, as described before, the SOI substrate in which the silicon single crystal wafer S is laminated on a back face of the underlying insulating film BOX. In this example, this silicon wafer is removed to make the pixel array portion transparent. Further, the switching TFT may be made of single crystal silicon without processing the steps A and B (not shown in the figure). Furthermore, a part of the single crystal silicon, which is disposed on a back face of the underlying insulating film BOX under a portion the pixel array, may be removed.

Figure 15 shows a variation of figure 14, where a metal lead for connection to a counter electrode is provided on a top face of the SOI substrate. As shown in the figure, the metal lead 200 is patterned over the intermediate insulating film 199 and the insulating film BOX is positioned under them. A resist 202 is patterned on the back face of the insulating film BOX so as to surround the metal lead 200. The insulating film BOX composed of silicon oxide material, and the intermediate insulating film 199, composed of PSG or else, are selectively etched away through the patterned resist using an etchant, composed of hydro-

fluoric acid or else, to thereby expose the back of the metal lead 200. In a later step, this exposed metal lead 200 will be electrically connected to a counter electrode which is formed on an internal surface of a counter substrate of a liquid crystal cell.

Figure 16 is a schematic step diagram showing a fifth example of the IC process. In a manner similar to figure 14, the SOI substrate is utilised to constitute a semiconductor device for a light valve. A pixel array will be formed on a right half portion of the figure, and a drive circuit will be formed on a left half portion of the same figure. First in step A, a monosilicon layer S on an insulating film BOX is subjected to doping for forming a well, and to field doping. Thereafter a LOCOS process is applied to form a field oxide film 211. The field oxide film 211 entirely covers a portion where a pixel array is to be formed, while individually isolated device regions 212 are provided in another portion where a drive circuit is to be formed. Further, a thin oxide film 214 is formed over the device region 212. In step B, a patterned polysilicon thin film 213 is formed on the field oxide film 211. In addition, the thin oxide film 214 is removed from the device region 212. In step C, a silicon transistor 215 of the drive circuit and a TFT 216 for pixel switching are concurrently formed in a manner similar to the previous examples. Further, the polysilicon thin film 213 is partly extended to form a pixel electrode. In step D, the silicon transistor 215 and the TFT 216 are covered by an intermediate insulating film 217. Thereafter, a patterned metal lead 218 is formed over the film 217. Further, though not shown in the figure, a passivation film is coated over the metal lead 218. After bonding the transparent support substrate onto the surface of the substrate SOI with the transistors, the processing is switched to a back face of the substrate such that the back silicon wafer is entirely removed using the underlying insulating film BOX of the SOI substrate as an etching stopper. The etchant may be composed of an alkali KOH solution. At this stage, the pattern of the top face can be viewed from the back face through the transparent insulating film BOX. Consequently, a patterned resist 219 is formed directly on the back face of the BOX to selectively cover the drive circuit portion without using a two-face aligner. The insulating film BOX and the monosilicon layer S are further etched away through the resist 219 to thereby expose a back face of the field oxide film 211 positioned on the pixel array portion.

Figure 17 shows a variation of figures 16(D) but a thinned form. This variation has basically the same construction; however, a pixel array portion is not provided on a field oxide film, but is provided on a thin oxide film 220. In such a structure, a monosilicon layer S of the SOI substrate is etched away using the thin oxide film 220 as an etching stopper so that the monosilicon layer S is selectively removed from the pixel array portion. In this variation, the distance between a pixel electrode and a liquid crystal layer (not shown) is further reduced to more efficiently transmit a drive voltage to thereby improve an image display quality, as compared to the figure 16 structure.

The description will now turn to the etching process of the back face in conjunction with figures 18-25. The transparent support substrate disposed at the surface side and the adhesive layer are omitted from figures 18 to 25. The transparent support substrate disposed at the surface side and the adhesive layer are omitted from figures 18 to 25.

Figure 18 is a first example of the etching process in which a bulk monosilicon substrate is etched from a back face. First in step A of the preceding IC process, a stopper film 231 is provisionally formed on a top face of a silicon single crystal substrate S. The stopper film 231 may be composed of a silicon oxide film, a silicon nitride film or a composite film thereof. Though not shown in the figure, a pixel array is formed on the stopper film 231. On the other hand, a drive circuit is formed on another portion outside the stopper film 231. In the IC process, a patterned resist film 232 is provisionally formed on the back face of the monosilicon substrate Si. The resist film 232 may be composed of a silicon nitride film, and may be patterned by means of a two-face aligner. Subsequently in step B, after bonding adhesively the transparent support substrate onto the other surface of the single crystal S substrate (not shown in the figures), the monosilicon substrate S is etched away through the resist mask 232 to make the pixel array portion transparent.

The monosilicon substrate S is etched by a KOH solution to reach the stopper film 231. This example utilises the two-face aligner which rather complicates the preceding IC process. Further, the resist film 232 is rather easily damaged by scratching or other effect. In addition, the monosilicon substrate S normally has a bulk thickness in the order of 500-600 μm, thereby disadvantageously generating a great step or gap g. Such a steep step would hinder assembling of a liquid crystal cell in a later process.

Figure 19 is a schematic step diagram showing a second example of the etching process. In this example, as shown by step A, an epitaxial silicon substrate is adopted. An epitaxial layer 242 is provided on a silicon substrate 241. The epitaxial layer 242 has an impurity density set lower than that of the silicon substrate 241. For example, the silicon substrate 241 has an impurity density more than 1×10^{18} cm^{-3}, while the epitaxial layer 242 has an impurity density less than 1×10^{18} cm^{-3}. Next, in step B of the IC process, an impurity is selectively doped into a pixel array portion at a high density to turn the epitaxial layer into P+ type of N+ type: the same as the substrate 241. Further, a stopper film 243 is formed thereover. Then, though not shown in the figure, a pixel array and a drive circuit are concurrently formed by the IC proc-

ess. Thereafter the transparent support substrate is bonded adhesively onto a surface of the silicon substrate (not shown in the figures).

In the next step C, the etching process of the back face is conducted. This example utilises an etchant composed of a mixture of hydrofluoric acid, nitric acid and acetic acid to effect selective etching based on the impurity density difference. Namely, the above etchant substantially does not etch a low density impurity region, while the same etchant selectively etches a high density impurity region. Accordingly in step C, the silicon substrate 241 of the P+ or N+ type is entirely removed first, and then the high density epitaxial layer is likewise etched just under the stopper film 243. On the other hand, the P^- or N^- type epitaxial layer 242 formed with the drive circuit is left as it is without being etched.

Alternatively, the silicon substrate 241 may not be subjected to complete etching but the silicon substrate may be ground until an intermediate stage thereby speeding up the processing. As described above, the present example utilises the selective etching based on the difference in etching rates due to the difference in impurity density. The transparent pixel array can thus be realised without using the two-face aligner.

Further, only the low density epitaxial layer 242 is left in the last stage, thereby reducing the gap g.

Figure 20 is a schematic step diagram showing a third example of the etching process. As described above, the figure 19 method uses the epitaxial substrate to remove a bulk thickness of the back face by selective etching without using the two-face aligner. However, the epitaxial substrate is disadvantageously more expensive than a regular bulk monosilicon substrate. In view of this, the present example applies the selective etching technology to the bulk monosilicon substrate. First in step (A) of the IC process, a stopper film 251 is formed on a pixel array area. Further, a P type impurity is doped with a high density under the stopper film 251 within its border. Such doping can be effected by ion implantation which is effective to adjust a depth of a high density impurity region 252 by regulating acceleration energy. In this example, the region 252 has a depth in order of 10 μm. Thereafter the transparent support substrate is bonded adhesively onto a surface of the single crystal silicon substrate with the pixel area (not shown in the figures). In step (B), the monosilicon substrate S is ground from a back face to reduce its thickness to 10 μm. Next, the high density impurity region 252 is selectively etched away by using a solution containing hydrofluoric acid, nitric acid and acetic acid at the ratio of 1: 3 : 8. As a consequence, the pixel array can be made transparent without using the two-face aligner. Further, the gap g can be reduced to 10 μm.

Figure 21 is a schematic step diagram showing a fourth example of the etching process. This example also adopts the selective etching technology. However, an etchant composed of an alkali KOH solution is used in place of a solution of hydrofluoric acid, nitric acid and acetic acid. The KOH solution is blocked from etching by a silicon oxide film and a silicon nitride film. In addition, the etching reaction of the KOH solution is stopped by a B type high density impurity layer.

First, in step (A) of the IC process, a stopper film 262 is provisionally formed over a silicon single crystal substrate 261 to cover a pixel array area. Though not shown in the figure, a pixel switching TFT and other elements are formed on the stopper film 262 by the IC process. On the other hand, a silicon layer 263 is reserved on a drive circuit area in which transistor elements are integrally formed by the same IC process. In this example, a P type high density impurity layer 264 is buried just under the monosilicon layer 263. This burying process is conducted by ion implantation while adjusting the acceleration energy. Thereafter the transparent support substrate is bonded adhesively onto a surface of the single crystal silicon substrate (not shown in the figures). In next step (B), the silicon substrate 261 is removed and made transparent by using an etchant composed of KOH solution. As described before, the P type high density impurity layer 264 is hardly etched by the KOH solution, and is therefore left as it is. The high density impurity layer 264 which is left has a thickness in the order of several μm to thereby significantly reduce the gap g.

Figure 22 is a schematic step diagram showing a fifth example of the etching process. In step (A) of the IC process, a stopper film 272 is formed on a top face of a monosilicon substrate 271. Though not shown in the figure, thereafter a drive circuit and a pixel array are formed integrally by the IC process. Thereafter the transparent support substrate is bonded adhesively onto a surface of the single crystal silicon substrate (not shown in the figures). In next step (B) the back face is processed. First, a silicon substrate 271 is thinned to a given thickness in the order of, for example, 2 μm by back face grinding such that the pattern on the top face can be viewed from the back face. Consequently, a patterned resist 273 is formed on the ground back face of the silicon substrate 271 to selectively cover the drive circuit portion without using a two-face aligner. In this example, the resist film 273 is composed of a photo-sensitive fluorocarbon resin which has a good chemical resistance to the KOH solution. Subsequently in step (C), the KOH solution is applied to remove a bulk thickness of the ground silicon substrate under the stopper film 272. In this example, the gap g can be further reduced to the order of 2 μm.

Figure 23 is a schematic step diagram showing a sixth example of the etching process. In step (A), a bulk thickness of a monosilicon substrate 281 is removed by a KOH solution to make transparent a por-

tion under a stopper film 282 in a manner similar to step (B) of the figure 18 method. As described before, at this stage, the silicon substrate 281 which is left has a thickness in the order of 500 μm so that the gap g is still great. This relatively large gap g would hinder the assembly of a liquid crystal cell. Thus in order to thin the bulk thickness which is left, a back face of the silicon substrate is entirely coated by a protective film 283 in step (B). This protective film 283 may be composed of silicon rubber. Next in step (C), the back face of the substrate is ground so that the thickness of the silicon substrate 281 is reduced in the order of 20 μm. Lastly in step (D), the protective film 283 is removed.

Figure 24 is a schematic step diagram showing a seventh example of the etching process. In step (A) of the preceding IC process, a stopper film 292, composed of silicon oxide, is provisionally formed over a top face of a single crystal silicon substrate 291 within a pixel array area. Further, a drive circuit is integrally formed, and concurrently posts 293, composed of silicon oxide, are buried in the drive circuit portion. The burying depth is in the order of 5-10 μm. For example, after forming trenches, the silicon oxide is deposited to fill the trenches. Thereafter the transparent support substrate is adhesively bonded onto a surface of the single crystal silicon substrate (not shown in the figures). In next step (B), rough grinding is applied to a back face of the single crystal silicon substrate 291 and then mechanical chemical polishing is carried out. The mechanical chemical polishing features an extreme selection rate of 1 to 1000 or more between SiO_2 and Si, such that the bulk thickness of the silicon substrate can be selectively removed under the stopper film 292. Further, since the silicon oxide posts or columns 293 are buried selectively close to each other, silicon around the posts is also left for avoiding any ill affect to the drive circuit disposed on the top face.

Figure 25 is a schematic step diagram showing an eighth example of the etching process. In this example, a SOL substrate is subjected to the etching process. First, in step (A) of the preceding IC process, a stopper film 301 is formed in a top face of the SOI substrate. This SOI substrate is composed of a laminate of a back silicon wafer 302, a top monosilicon layer 303 and an intermediate insulating film 304. Though not shown in the figure, a pixel array is formed on the stopper film 301, while a drive circuit is formed in the remaining portion of the SOI substrate. Preferably, the monosilicon layer 303 has a relatively great thickness in the order of 1.5 to 2 μm or more so as to stabilise the operating characteristics of the drive circuit. Moreover, this thickness of 1.5-2 μm may be utilised to determine a gap spacing of a liquid crystal cell. Thereafter the transparent support substrate is bonded adhesively onto a surface of the substrate SOI (not shown in the figures). In next step (B), the silicon wafer 302 is entirely removed using the intermediate insulating film 304 as an etching stopper. Subsequently in step (C), a patterned resist 305 is formed on a back face of the intermediate insulating film (BOX) 304 in registration with the drive circuit portion. At this stage, since the silicon crystal layer 303 has a thickness in the order of 1.5-2 μm, a pattern of the top face can be viewed from the back face to thereby enable correct patterning of the resist 305 without using a two-face aligner. Lastly in step (D), the intermediate insulating film 304 and the monosilicon layer 303 are etched through the resist 305 to expose a portion under the stopper film 301. In this case, the gap g may be finally reduced to the order of 2 to 5 ± 0.5 μm.

As described above, according to the present invention, the semiconductor device for a light valve is comprised of a semiconductor substrate having a thick opaque portion and a thin transparent portion, a pixel array formed in the transparent portion, a drive circuit formed in the opaque portion, and a transparent support substrate laminated to a top major face of the semiconductor substrate. In such a construction, an IC fabrication process is applied to the semiconductor substrate, composed of bulk monosilicon, so as to concurrently form the pixel array and the drive circuit. Consequently, a drive circuit which is faster and as a higher operation can be realised without increasing the processing steps. Further, after forming the pixel array and the drive circuit in the semiconductor substrate and laminating the transparent support substrate onto the top face of the semiconductor substrate, a bulk thickness of the semiconductor substrate is removed by etching from an area just under the pixel array to thereby quite easily make the pixel array portion transparent. Further, since a portion formed with the drive circuit has a thickness or bulk of the semiconductor substrate, the heat generated by the drive circuit can be absorbed immediately, so that the drive circuit operates stably.

The aforegoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.

Claims

1. A semiconductor device for a light valve comprising

   a substrate (3) having an opaque portion and a transparent portion,

   a pixel (9) formed on the transparent portion,

   a drive circuit (8) formed on the opaque portion for driving the pixel,

   characterised by

   a transparent support substrate (5) lamin-

ated to the substrate over at least the pixel.

2. A semiconductor device as claimed in claim 1, in which the semiconductor substrate has a monocrystalline silicon layer, and the drive circuit comprises a semiconductor integrated circuit formed in the major face of the monocrystalline silicon layer.

3. A semiconductor device as claimed in claim 1, in which the semiconductor substrate comprises an SOI wafer having a stacked-structure of a silicon plate and a monocrystalline silicon layer interposed with an insulating film.

4. A semiconductor device as claimed in claim 2 or 3, in which said opaque portion is formed by the semiconductor substrate being thicker relative to said transparent portion which is relatively thin.

5. A semiconductor device as claimed in any one of claims 1 to 4, in which there is a plurality of pixels arranged in an active matrix array having pixel electrodes arranged in a matrix and switching elements of the respective drive circuit for selectively driving individual pixel electrodes.

6. A semiconductor device as claimed in claim 5, in which each switching element comprises any one of a polycrystalline silicon thin film transistor, an amorphous silicon thin film transistor, or a monocrystalline silicon thin film transistor.

7. A semiconductor device as claimed in claim 6, in which the polycrystalline silicon thin film transistor is formed in a polycrystalline silicon thin film and the pixel electrode is made of the polycrystalline silicon thin film having a thickness in order of 50nm ± 10nm.

8. A semiconductor device according to any one of the preceding claims, in which the or each drive circuit and the or each pixel comprises concurrently formed field effect type transistors including a field oxide film, a gate oxide film, a gate electrode, a source region and drain region.

9. A semiconductor device as claimed in any one of the preceding claims, in which the semiconductor substrate has an insulating film (13) disposed as an etching stopper on the transparent portion.

10. A semiconductor device as claimed in claim 9, in which a thickness of the insulating film in a region where the pixel is formed is smaller than of the insulating film in a region where the drive circuit is formed.

11. A semiconductor device according to any one of the preceding claims, in which the transparent support substrate is made of a transparent inorganic material having a thermal expansion coefficient comparable to that of the semiconductor substrate.

12. A semiconductor device as claimed in claim 11, in which the transparent inorganic material is at least one of a glass, a quartz or sapphire.

13. A semiconductor device as claimed in any one of the preceding claims, further including an adhesive layer (17) interposed between the transparent support substrate and the semiconductor substrate.

14. A semiconductor layer as claimed in any one of the preceding claims, further including a levelling layer (20) interposed between the adhesive layer and the semiconductor substrate.

15. A semiconductor device as claimed in claim 13 or 14, in which the adhesive layer and the levelling layer constitute the transparent support substrate.

16. A semiconductor device as claimed in any one of the preceding claims, in which the transparent portion has a cavity for receiving a counter substrate (16) so as to construct a light valve.

17. A semiconductor device as claimed in any one of the preceding claims, in which the semiconductor substrate has a light shielding film (84) disposed in registration with at least a part of the drive circuit.

18. A method of producing a semiconductor device for a light valve characterised by: forming a pixel (9) and a drive circuit (8) on a major face of a semiconductor substrate (3); laminating a transparent support substrate (5) on the major face of the semiconductor substrate; and selectively removing a thickness of the semiconductor substrate from a back face opposite to the major face over a portion in registration with the pixel.

19. A method of producing a semiconductor device as claimed in claim 18, in which forming the pixel and drive circuit includes forming an underlying stopper film (13) on the major face of the semiconductor substrate in registration with the pixel, and removing the thickness includes etching a back face of the semiconductor substrate to remove the thickness thereof to reach the stopper film.

20. A method of producing a semiconductor device as claimed in claim 19, in which forming the pixel and drive circuit includes forming a first region having a relatively high etching rate in a portion of the semiconductor substrate disposed under the stopper film, and a second region having a relatively low etching rate in another portion of the semiconductor substrate disposed outside the stopper film, and removing the thickness includes applying selective etching to the thickness of the semiconductor substrate, which uses a differential etch rate.

21. A method of producing a semiconductor device as claimed in claim 20, in which the first region is composed of an impurity region having a density greater than that of the second region, and the selective etching is carried out using an etchant which is a mixture of hydrofluoric acid, nitric acid or acetic acid.

22. A method of producing a semiconductor device as claimed in claim 20, in which the second region is comprised of an impurity region having a density greater than that of the first region, and the selective etchant includes an alkali etching liquid.

23. A method of producing a semiconductor device as claimed in any one of claims 18 to 22, in which removing the thickness includes grinding.

24. A method of producing a semiconductor device as claimed in any one of claims 19 to 23, in which forming the pixel and drive circuit includes embedding a silicon oxide post (293) into the major face of the semiconductor substrate over a portion outside the stopper film, and removing the thickness includes etching the semiconductor substrate by mechanical-chemical polishing.

FIG. 1 (A)

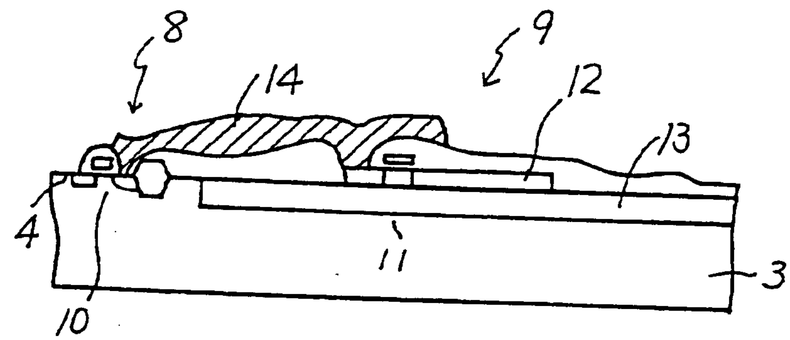


FIG. 1 (B)

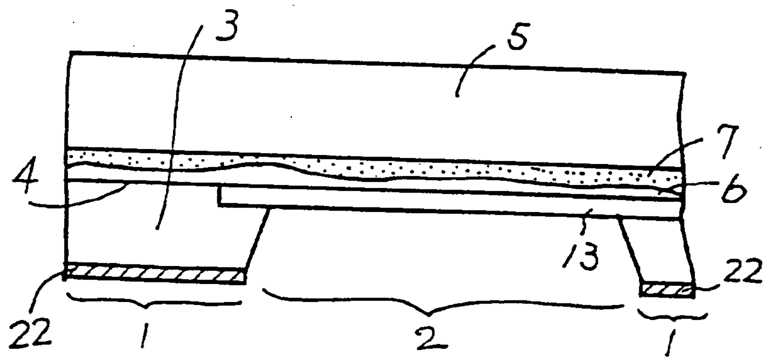


FIG. 1 (C)

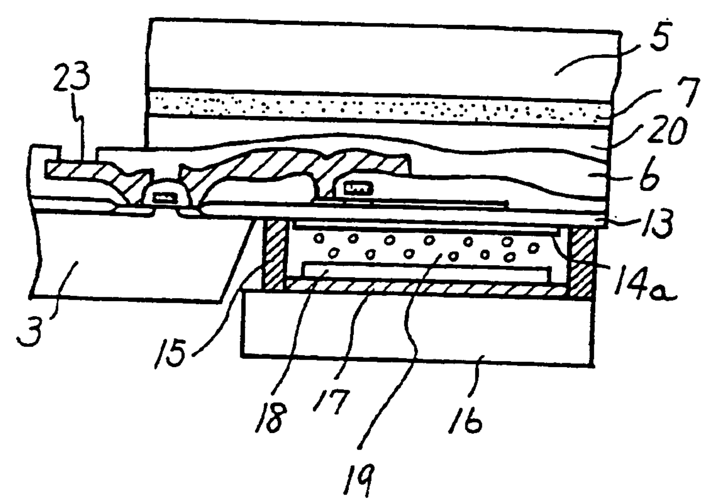


FIG. 2 (A)

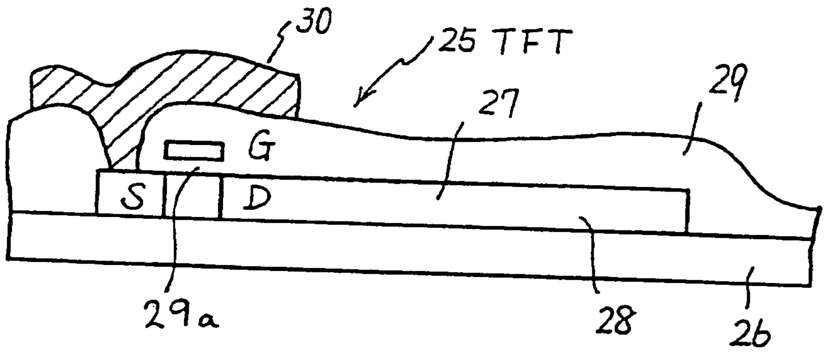


FIG. 2 (B)

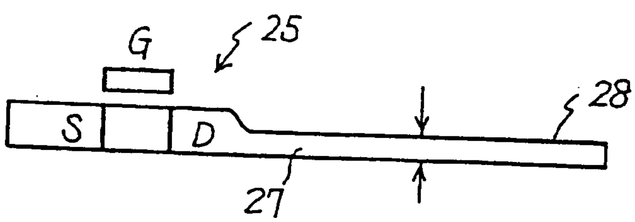


FIG. 3

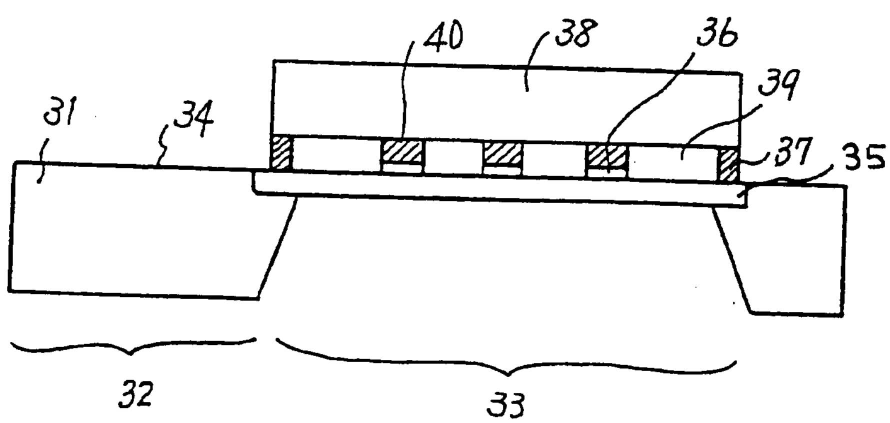


FIG. 4 (A)

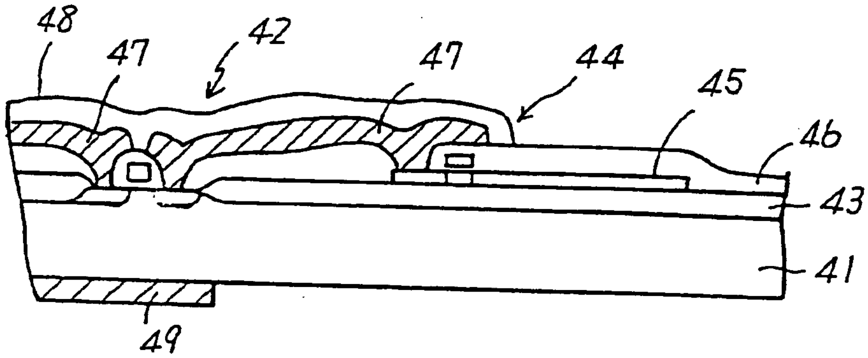


FIG. 4 (B)

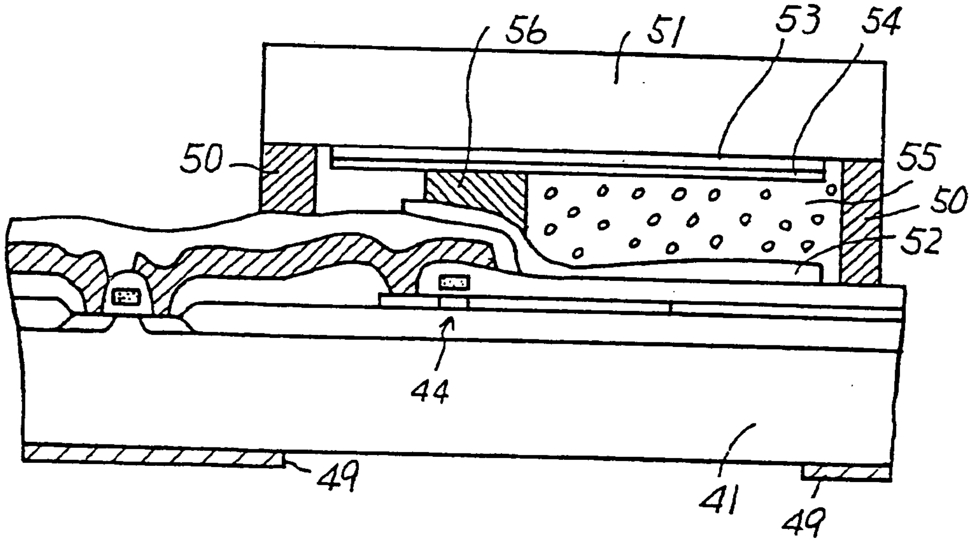


FIG. 4 (C)

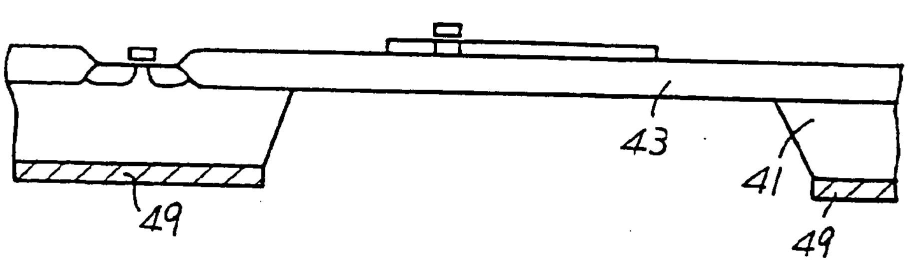


FIG. 5

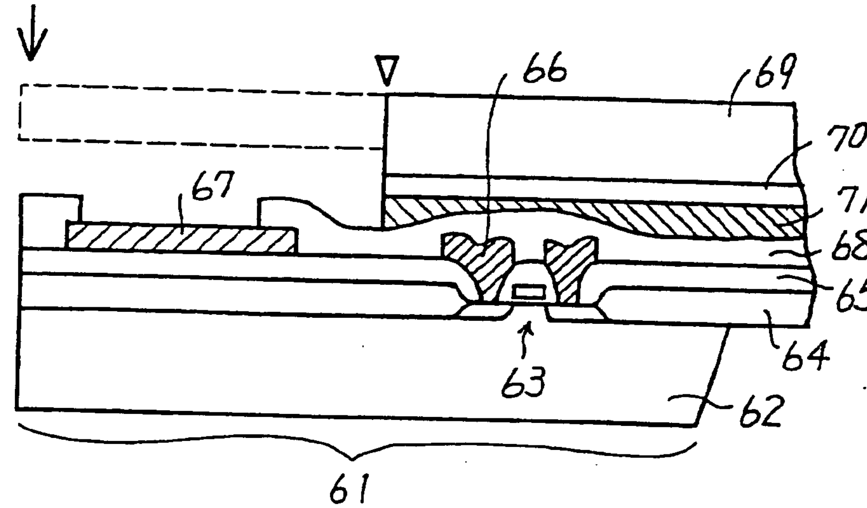


FIG. 6

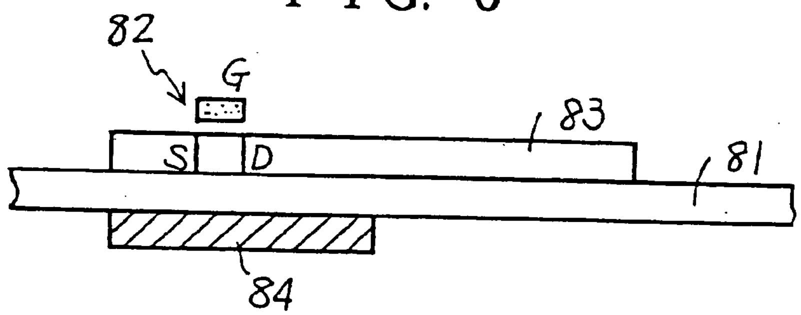


FIG. 7

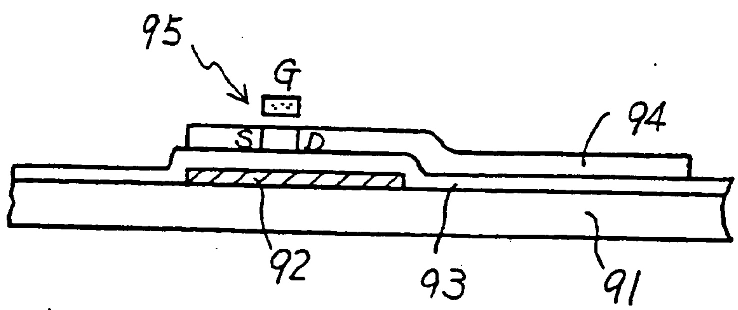


FIG. 8

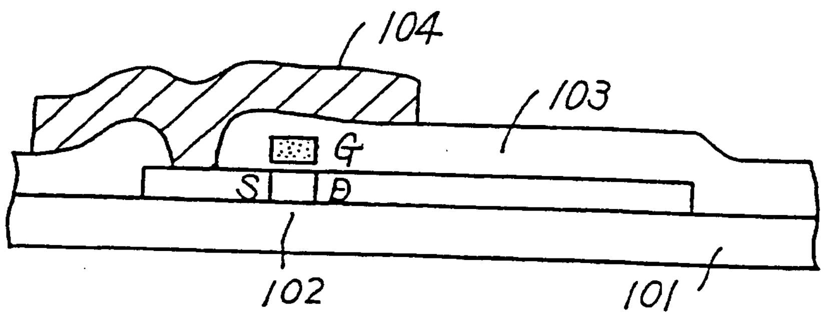


FIG. 9

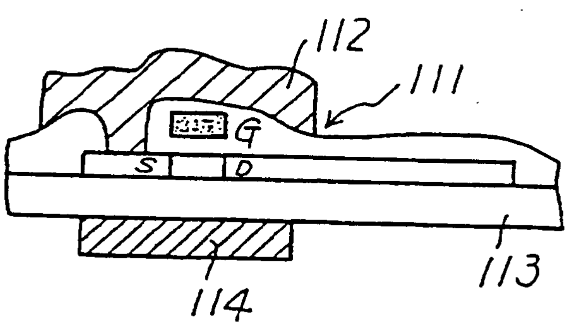


FIG. 10

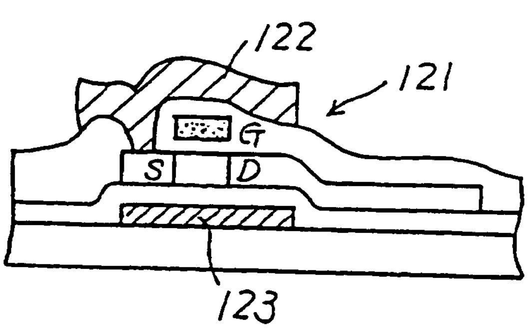


FIG. 11(A)

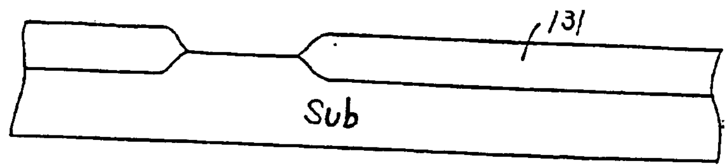


FIG. 11(B)

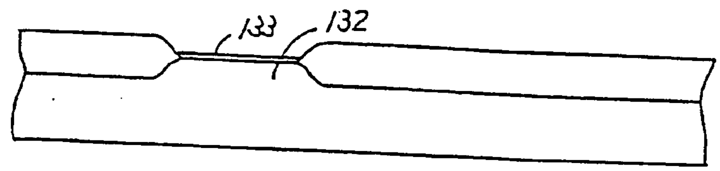


FIG. 11(C)

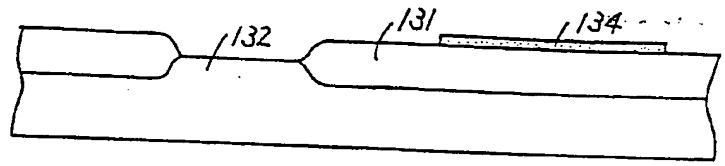


FIG. 11(D)

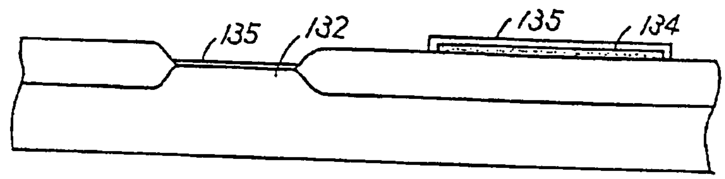


FIG. 11(E)

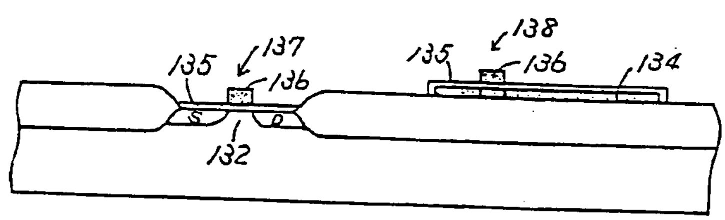


FIG. 11(F)

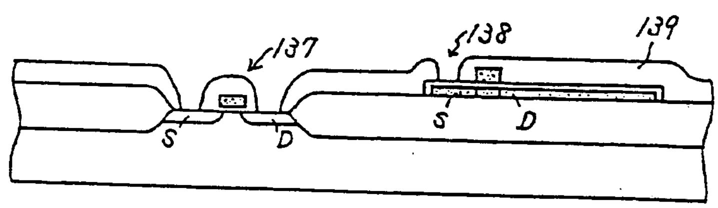


FIG. 11(G)

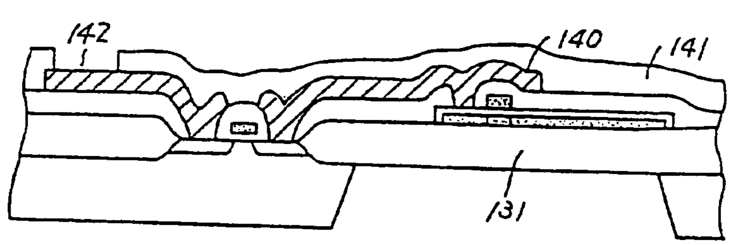


FIG. 12(A)

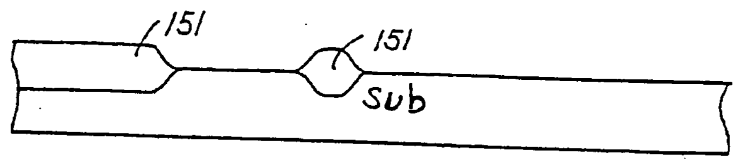


FIG. 12(B)

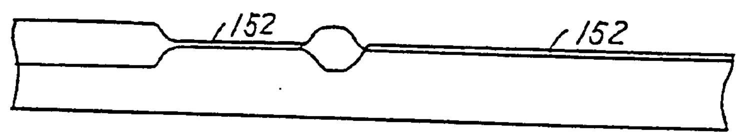


FIG. 12(C)

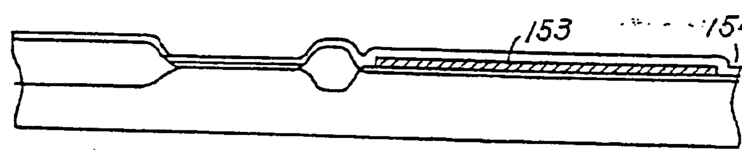


FIG. 12(D)

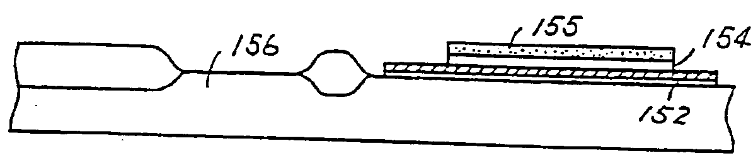


FIG. 12(E)

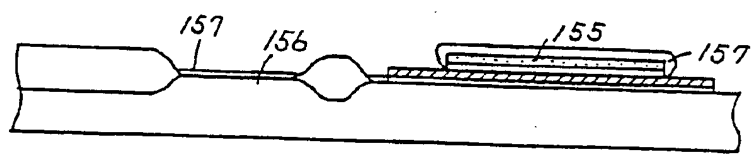


FIG. 12(F)

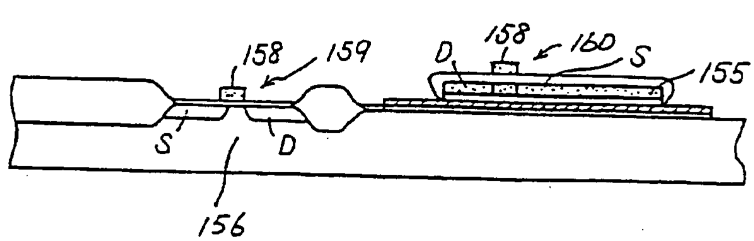


FIG. 12(G)

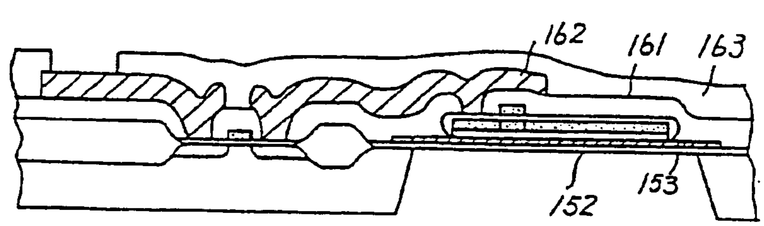


FIG. 13(A)

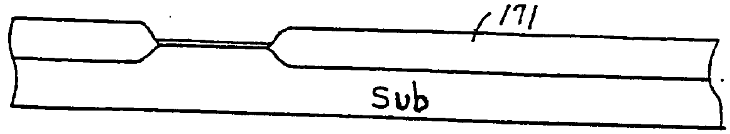


FIG. 13(B)

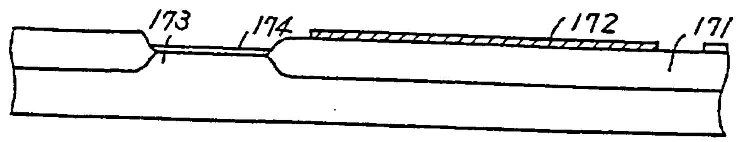


FIG. 13(C)

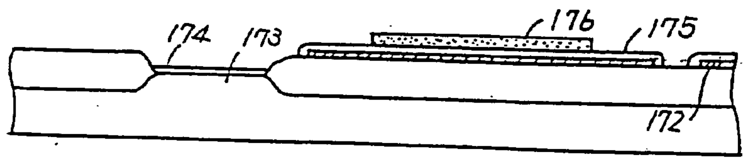


FIG. 13(D)

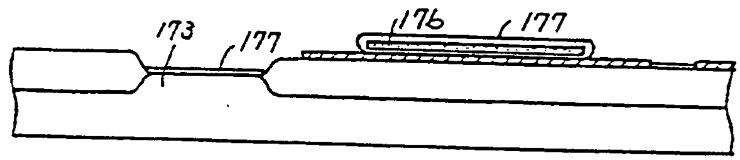


FIG. 13(E)

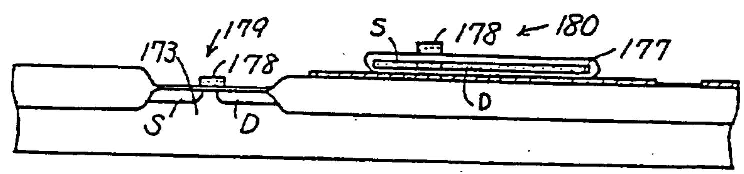


FIG. 13(F)

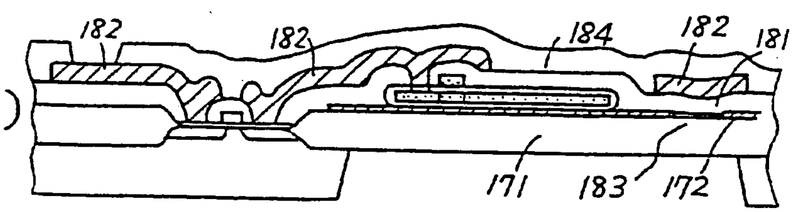


FIG. 13(G)

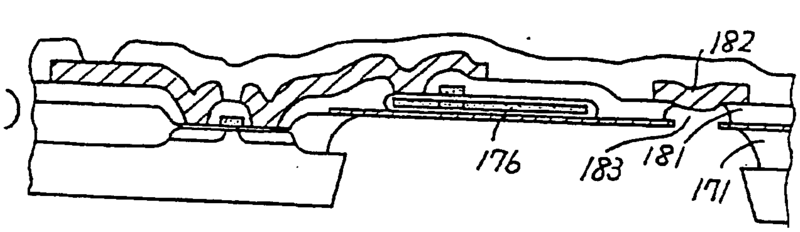


FIG. 14(A)

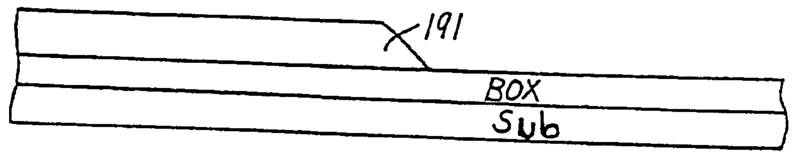


FIG. 14(B)

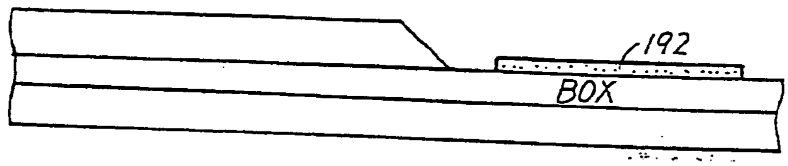


FIG. 14(C)

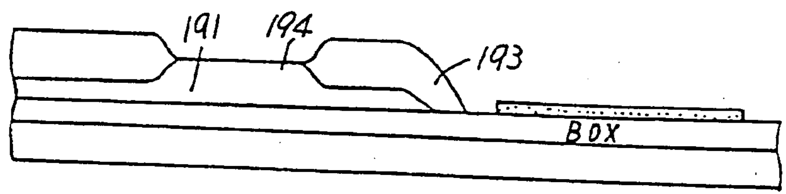


FIG. 14(D)

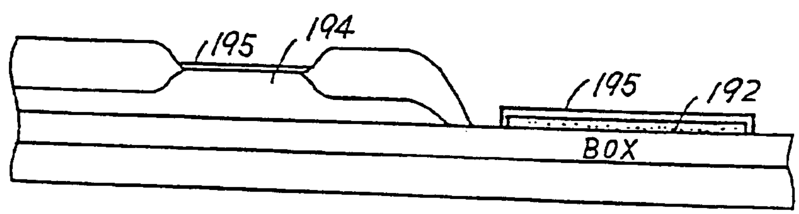


FIG. 14(E)

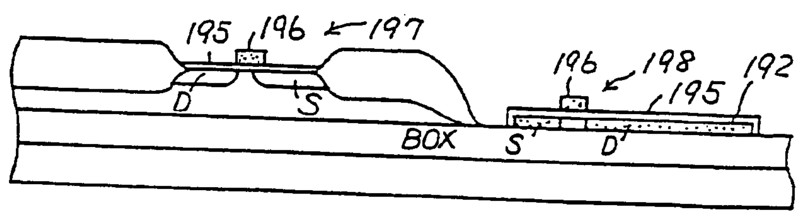


FIG. 14(F)

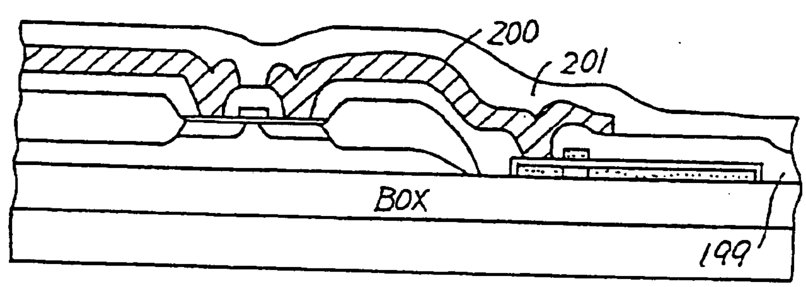


FIG. 15

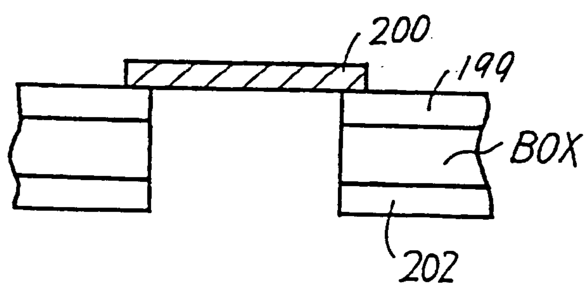


FIG. 16(A)

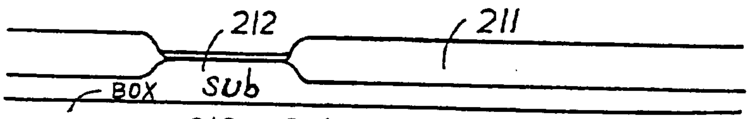


FIG. 16(B)

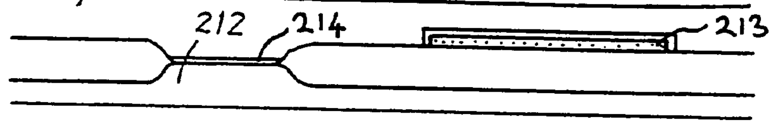


FIG. 16(C)

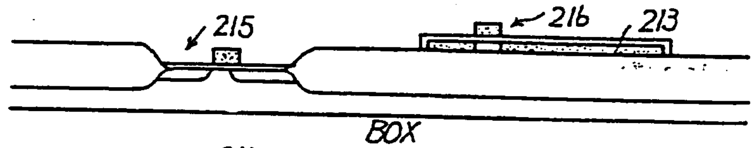


FIG. 16(D)

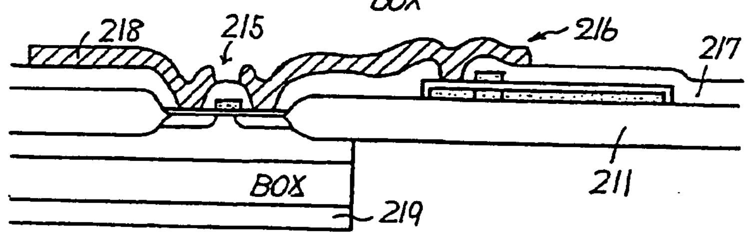
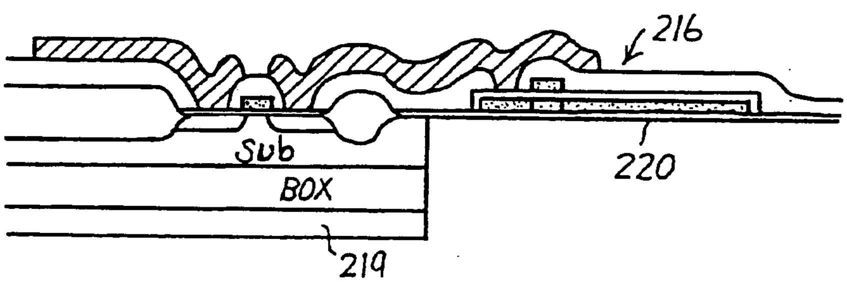


FIG. 17



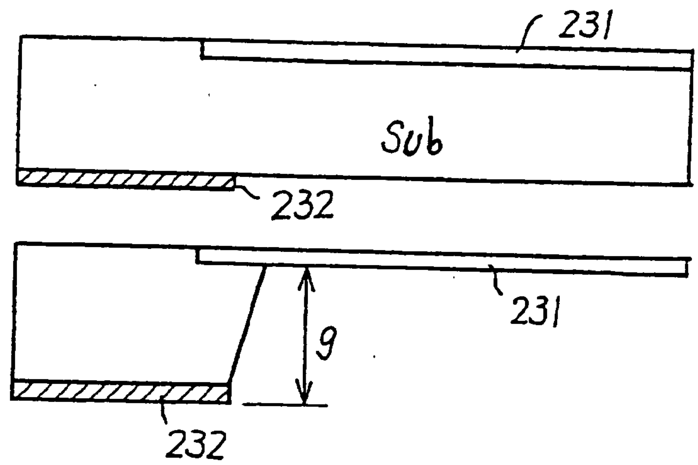


FIG. 18(A)

FIG. 18(B)

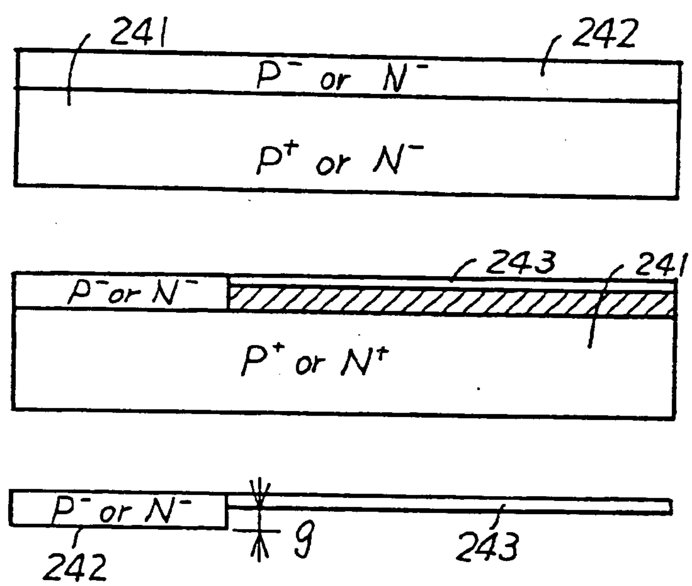


FIG. 19(A)

FIG. 19(B)

FIG. 19(C)

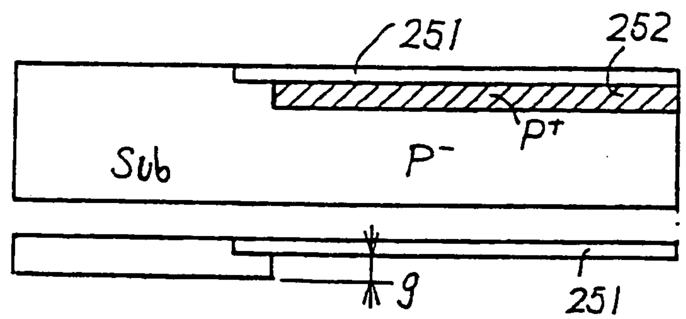


FIG. 20(A)

FIG. 20(B)

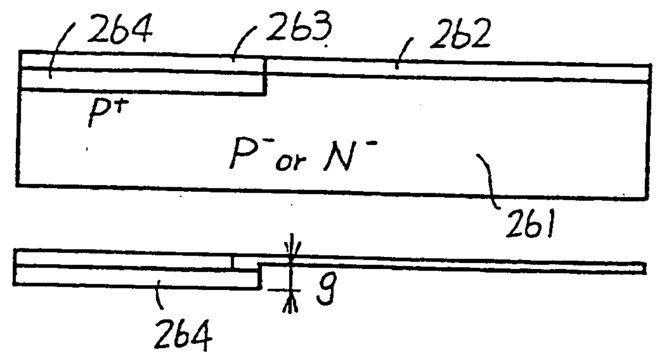


FIG. 21(A)

FIG. 21(B)

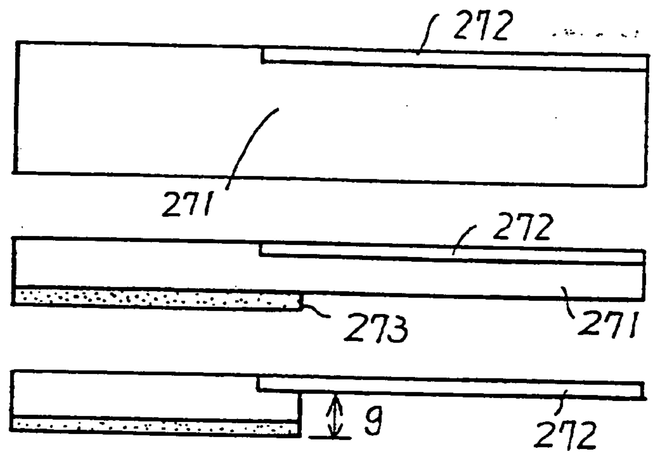


FIG. 22(A)

FIG. 22(B)

FIG. 22(C)

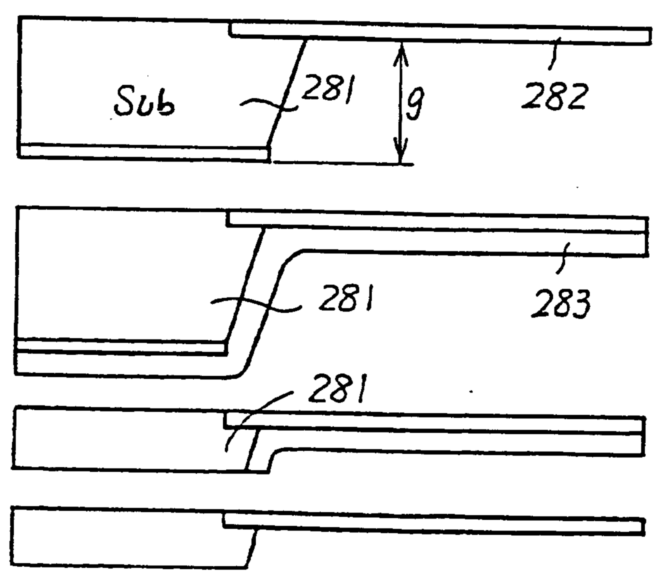


FIG. 23(A)

FIG. 23(B)

FIG. 23(C)

FIG. 23(D)

FIG. 24(A)

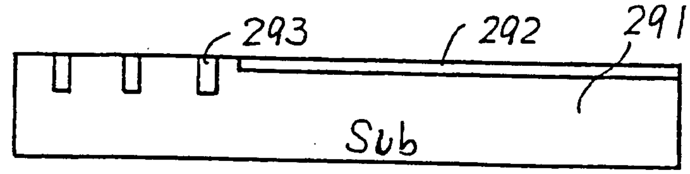


FIG. 24(B)

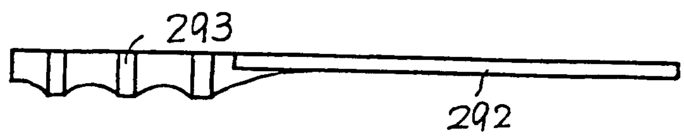


FIG. 25(A)

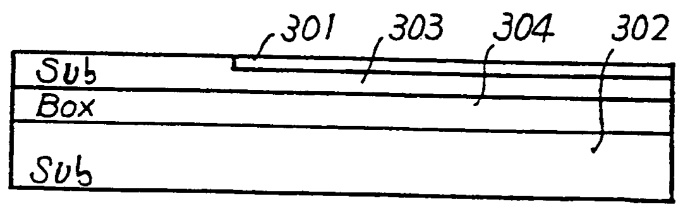


FIG. 25(B)

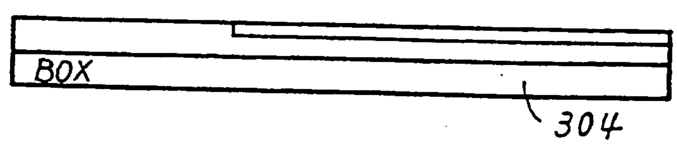


FIG. 25(C)

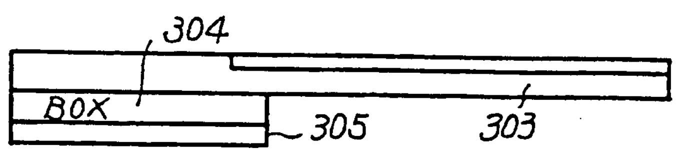


FIG. 25(D)

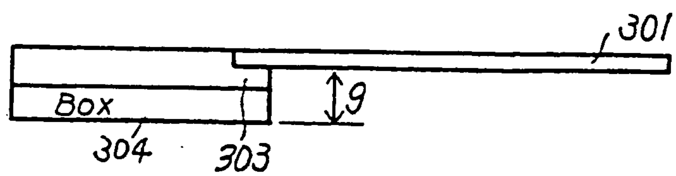


FIG. 26
PRIOR ART

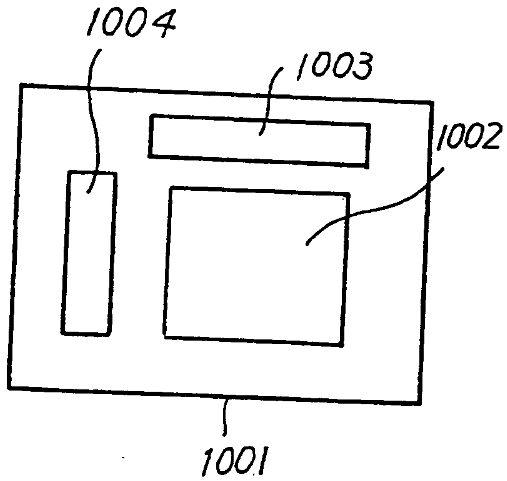
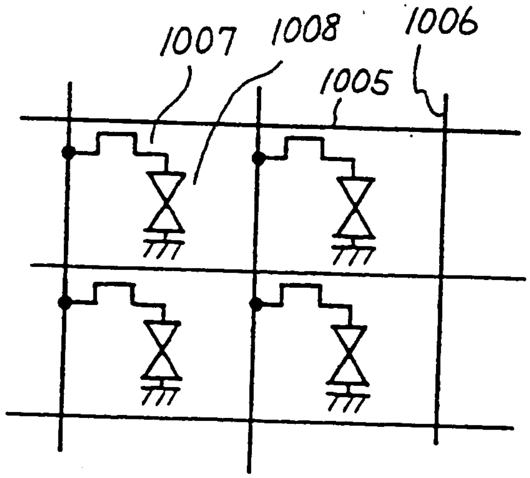


FIG. 27
PRIOR ART



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 6571

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
D,X	PATENT ABSTRACTS OF JAPAN vol. 15, no. 287 (P-1229)22 July 1991 & JP-A-03 100 516 (SHARP) 25 April 1991 * abstract * ---	1,2,5,6,8,16	G02F1/136 H01L27/12
A	EP-A-0 486 318 (SEIKO INSTRUMENTS) * column 19, paragraph 3 - column 23, paragraph 1; figures 11-15 * * column 26, paragraph 2 -paragraph 3 * ---	1-3,5,8,9,11,12,18,19	
A	PATENT ABSTRACTS OF JAPAN vol. 10, no. 1 (E-371)7 January 1986 & JP-A-60 167 364 (MATSUSHITA) 30 August 1985 * abstract * ---	1,13,14,18	
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 578 (E-864)20 December 1989 & JP-A-01 241 862 (SONY) 26 September 1989 * abstract * -----	1,5-7	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)
G02F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23 November 1993	WONGEL, H

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